ABSTRACT OF THE DISCLOSURE

On a basic measurement unit arranged in a lattice shape on a chip, a resistance measurement circuit, a capacity measurement circuit, an n-type MOS transistor measurement circuit, a p-type MOS transistor measurement circuit, and a ring oscillator measurement circuit are mounted by several tens of patterns. Each measurement circuit mounted by several tens of patterns is connected to a measurement bus to constitute a measurement bus net in accordance with measured items. Switching of connection of the measurement bus net with a measurement terminal pad is electrically controlled properly by X, Y address selection signals outputted from X, Y address decoders to X, Y address selection signal lines.